

ASMEX.186DV1



COPY OF PAPERS
ORIGINALLY FILED

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Raaijmakers et al.

Appl. No. : 09/764,711

Filed : January 18, 2001

For : METHOD OF DEPOSITING
SILICON WITH HIGH STEP
COVERAGE

Examiner : Roman, A.

) Group Art Unit 2812

) I hereby certify that this correspondence and all
) marked attachments are being deposited with
) the United States Postal Service as first-class
) mail in an envelope addressed to:
) Commissioner for Patents, Washington, D.C.
) 20231, on

) January 24, 2002

) (Date)

) Adeel S. Akhtar, Reg. No. 41,394

RESPONSE TO OFFICE ACTION

Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

In response to the Office Action mailed on October 24, 2001, please amend the above-captioned application as follows:

IN THE CLAIMS:

Please amend Claim 33 as indicated below:

33. (Amended) An integrated capacitor formed in a trench having a width of no more than about 0.25 μm and an aspect ratio greater than about 20:1, comprising:
a dielectric layer lining the trench; and
a conductively doped, as-deposited polysilicon layer filling the trench.

REMARKS

Claim Objections

The Examiner has objected to Claim 33, suggesting that "in trench" should be replaced with --in a trench--. Applicants have corrected Claim 33 accordingly. Accordingly, Applicants submit that the objection is overcome.